NPN SILICON PLANAR EPITAXIAL TRANSISTORS

BC817
BC818

SOT-23

SOT-23
SMD Package
RoHS compliant

FEATURES:

1. Marking
   BC817 = 6D
   BC817-16 = 6A
   BC817-25 = 6B
   BC817-40 = 6C
   BC818 = 6H
   BC818-16 = 6E
   BC818-25 = 6F
   BC818-40 = 6G
2. This product is available in AEC-Q101 Qualified and PPAP Capable also.
   Note: For AEC-Q101 qualified products, please use suffix -AQ in the part number while ordering.

APPLICATION: General-purpose switching and amplification

ABSOLUTE MAXIMUM RATING (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	BC817	BC818	UNIT
Collector–emitter voltage (V_{BE} = 0)	V_{CES}	50	30	V
Collector–emitter voltage (open base) I_C = 10mA	V_{CEO}	45	25	V
Emitter–base voltage (open collector)	V_{EBO}	5	5	V
Collector current (d.c.)	I_C	500		mA
Collector current (peak value)	I_{CM}	1000		mA
Emitter current (peak value)	I_{EM}	1000		mA
Base current (d.c.)	I_B	100		mA
Base current (peak value)	I_{BM}	200		mA
Total power dissipation up to T_{amb} = 25°C	P_{tot}	250		mW
Storage temperature	T_{stg}	-55 to +150		°C
Junction temperature	T_j	150		°C
Transition frequency at f = 100 MHz (I_C = 10mA; V_{CE} = 5V)	f_T	100		MHz
Thermal Resistance From junction to ambient	$R_{th\ j-a}$	500		K/W

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Collector cut–off current		I_{CBO}	I_E = 0; V_{CB} = 20V; T_j = 25°C	--	--	100	nA
			I_E = 0; V_{CB} = 20V; T_j = 150°C	--	--	5	µA
Emitter cut–off current		I_{EB0}	I_C = 0; V_{EB} = 5V	--	--	10	µA
Base−Emitter On Voltage		$V_{BE(on)}$	I_C = 500mA; V_{CE} = 1V	--	--	1.2	V
Collector Emitter Saturation voltage		$V_{ce(sat)}$	I_C = 500mA; I_B = 50mA	--	--	700	mV
D.C. current gain		h_{FE}	I_C = 500mA; V_{CE} = 1V	40	--	--	
D.C. current gain	BC817/BC818		I_C = 100mA;V_{CE}= 1V	100	--	600	
	BC817–16			100	--	250	
	BC818–16						
	BC817–25			160	--	400	
	BC818–25						
	BC817–40			250	--	600	
	BC818–40						
Transition frequency at f = 100 MHz		f_T	I_C = 10mA; V_{CE} = 5V	--		100	MHz
Collector capacitance at f = 1 MHz		Cc	I_E = Ie = 0; V_{CB} = 10V	--	5	--	pF

TYPICAL CHARACTERISTICS CURVES

Fig 1: DC Current Gain vs. Collector Current

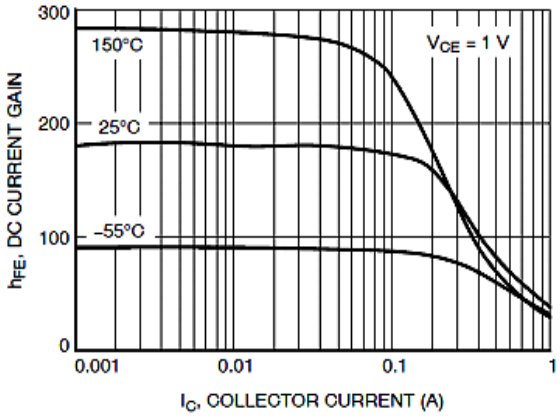


Fig 2: Collector Emitter Saturation Voltage vs. Collector Current

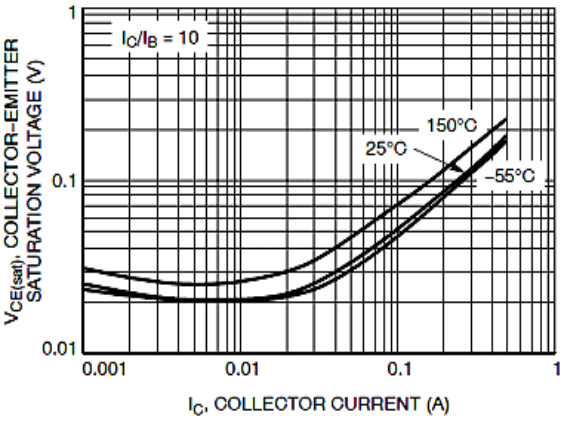


Fig 3: Base Emitter Saturation Voltage vs. Collector Current

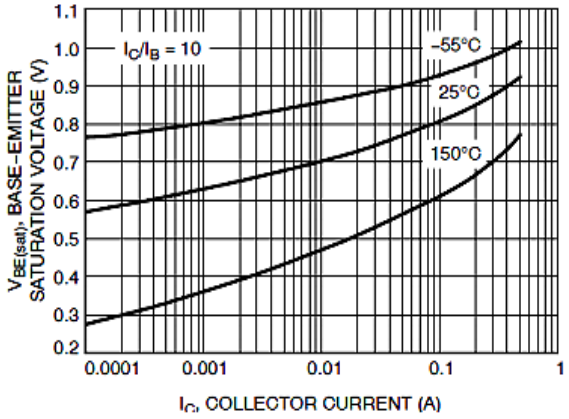


Fig 4: Base Emitter Voltage vs. Collector Current

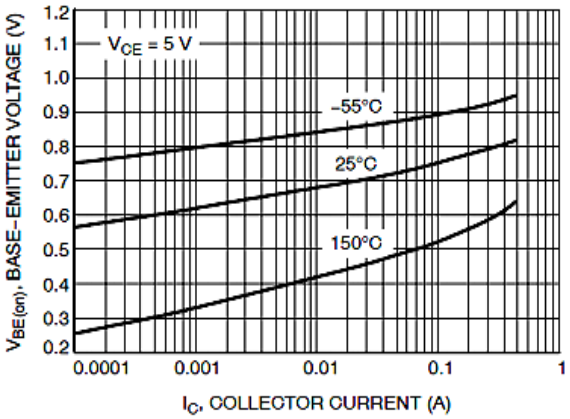


Fig 5: Current Gain Bandwidth Product vs. Collector Current

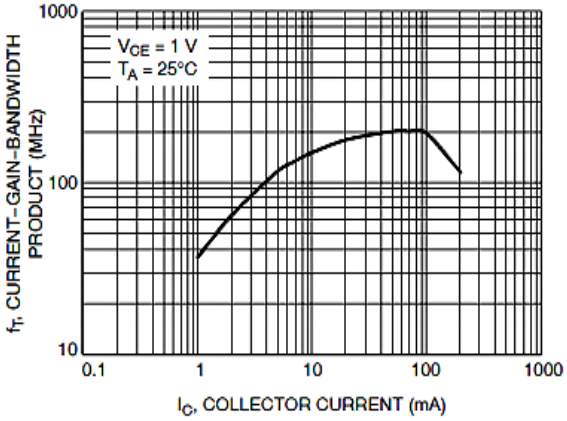
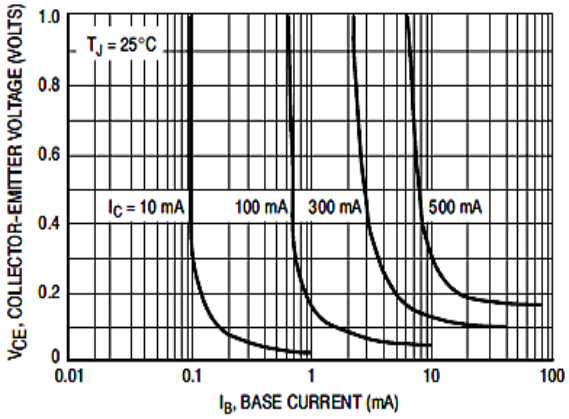


Fig 6: Saturation Region



TYPICAL CHARACTERISTICS CURVES

Fig 7: Temperature Coefficients

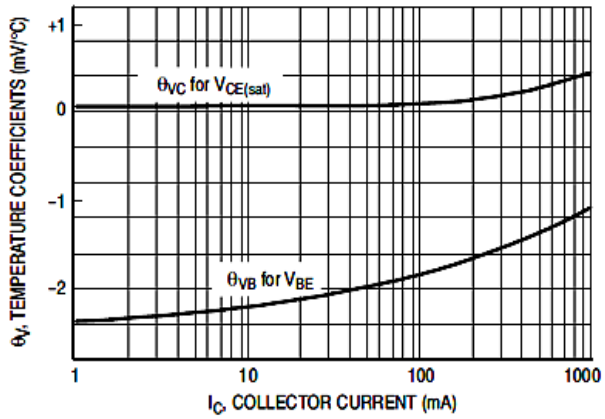


Fig 8: Capacitance

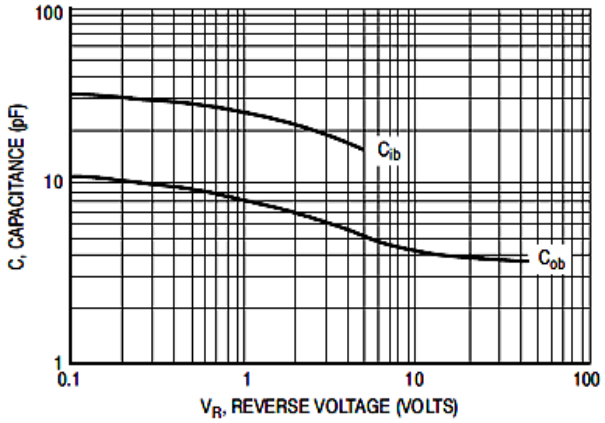


Fig 9: DC Current Gain vs. Collector

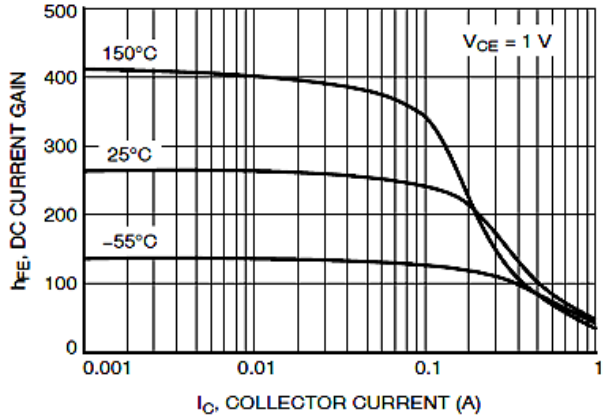


Fig 10: Collector Emitter Saturation Voltage vs. Collector Current

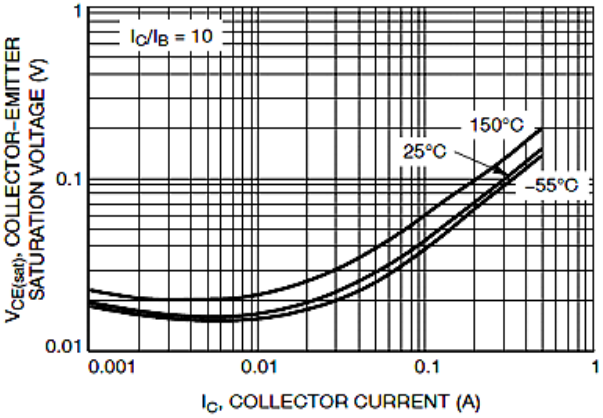


Fig 11: Base Emitter Saturation Voltage vs. Collector Current

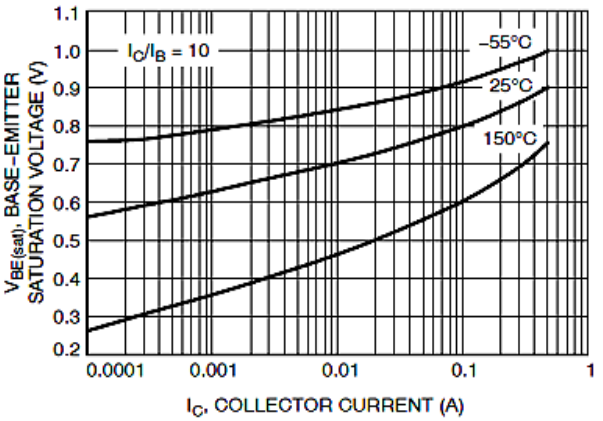
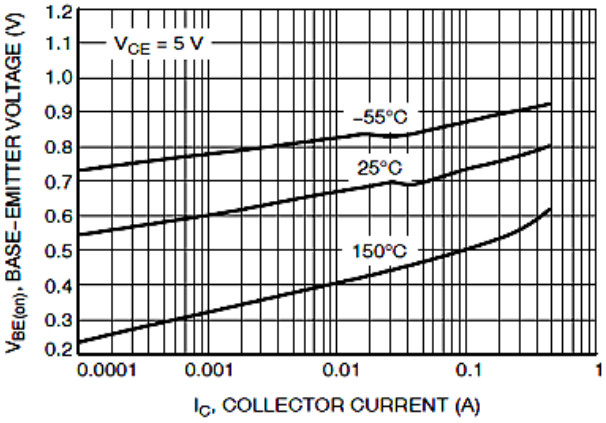


Fig 12: Base Emitter Voltage vs. Collector Current



TYPICAL CHARACTERISTICS CURVES

Fig 13: Current Gain Bandwidth Product vs. Collector Current

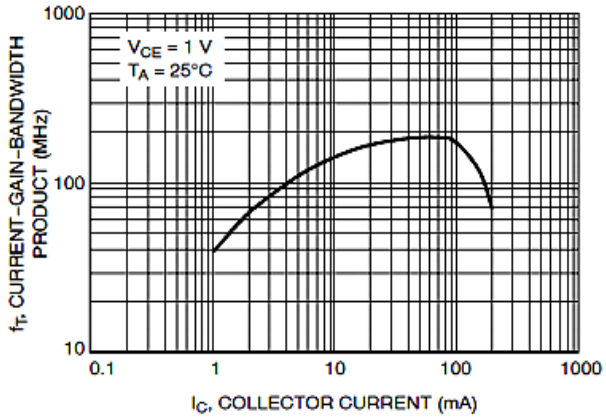


Fig 14: Saturation Region

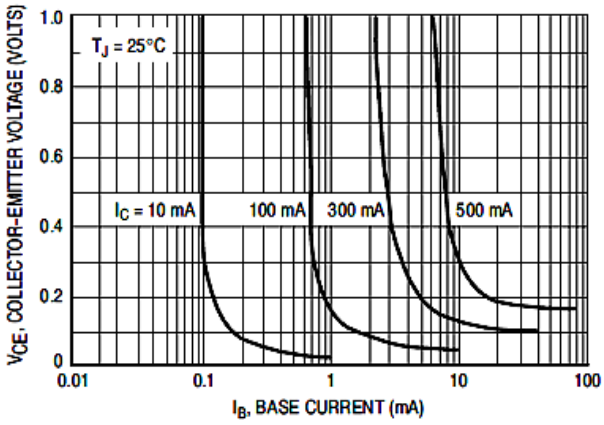


Fig 15: Temperature Coefficients

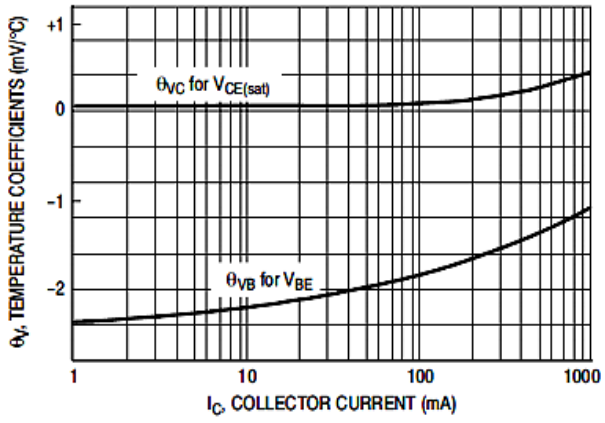


Fig 16: Capacitance

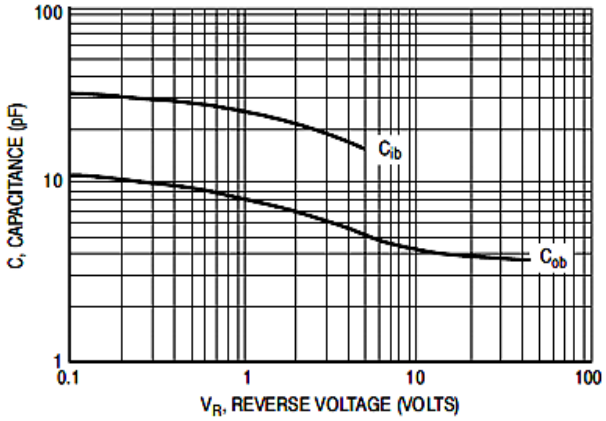


Fig 17: DC Current Gain vs. Collector Current

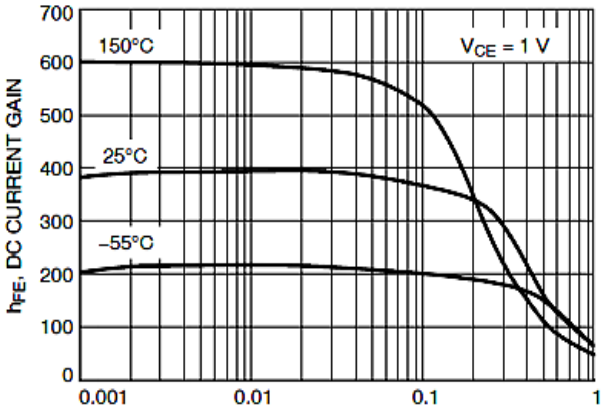
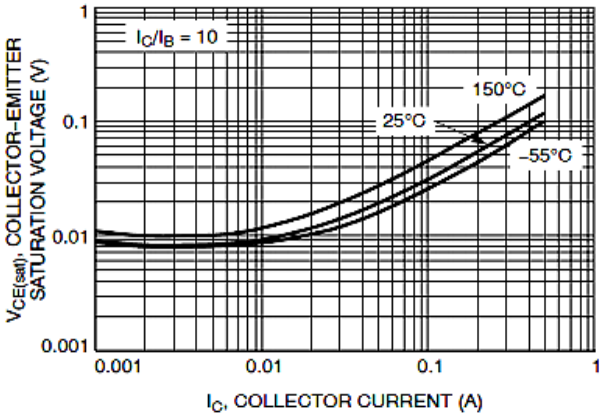


Fig 18: Collector Emitter Saturation Voltage vs. Collector Current



BC817_818
Rev04_18102024M

TYPICAL CHARACTERISTICS CURVES

Fig 19: Base Emitter Saturation Voltage vs.Collector Current

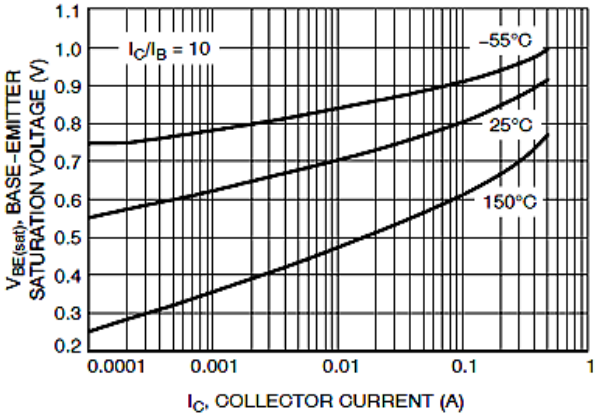


Fig 20: Base Emitter Voltage vs. Collector Current

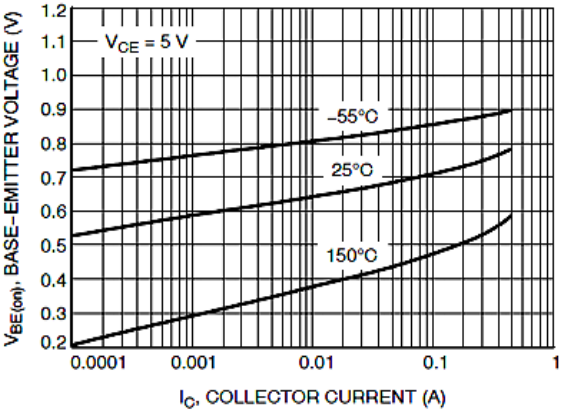


Fig 21: Current Gain Bandwidth Product vs. Collector Current

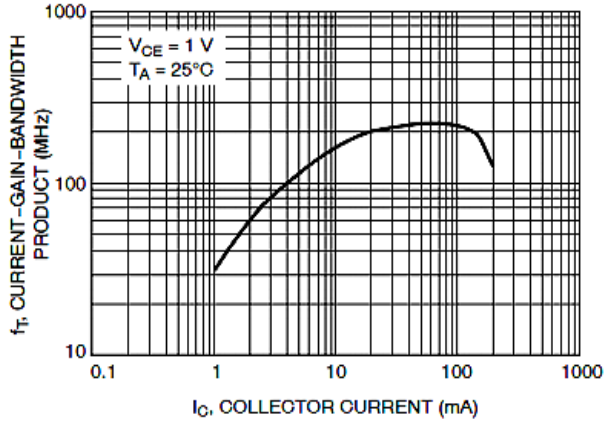


Fig 22: Saturation Region

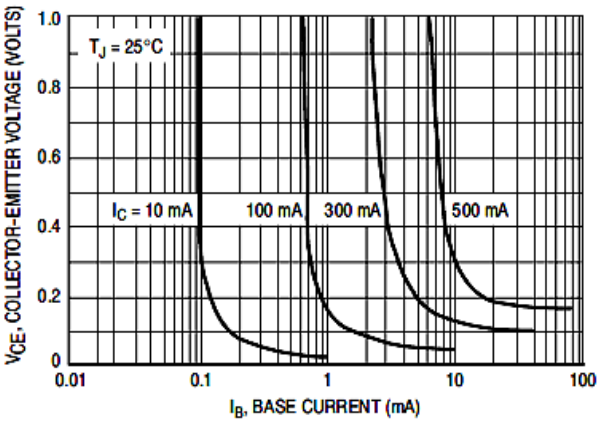


Fig 23: Temperature Coefficients

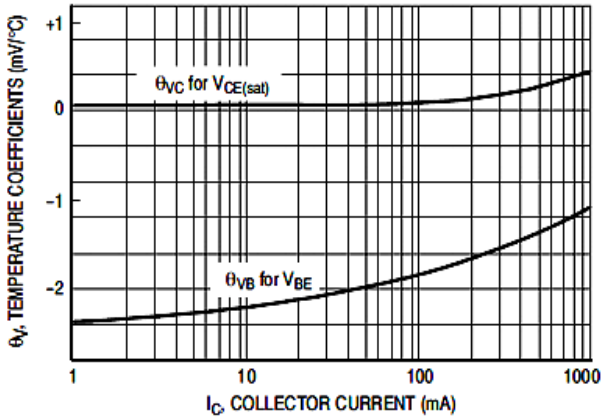
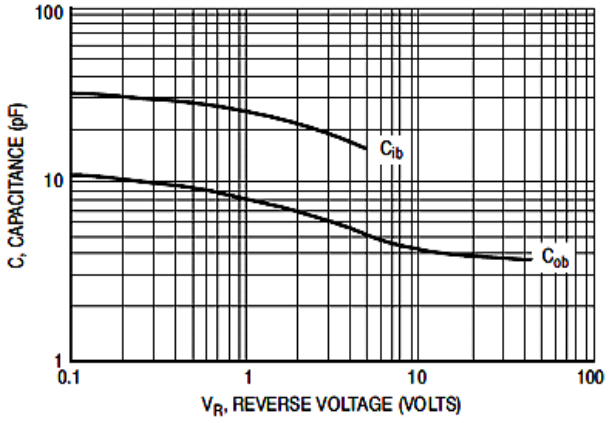


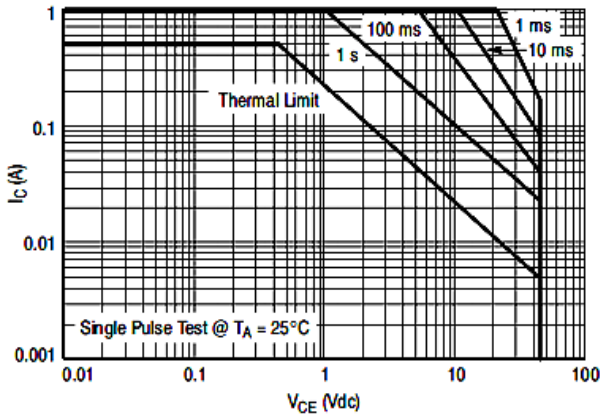
Fig 24: Capacitance



BC817_818
Rev04_18102024M

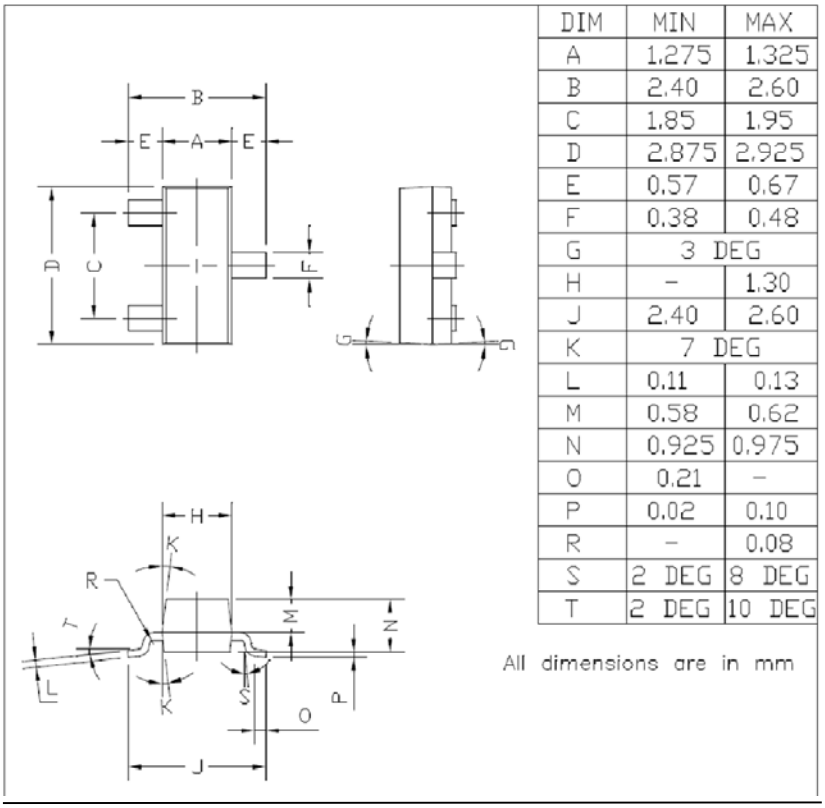
TYPICAL CHARACTERISTICS CURVES

Fig 25: Safe Operating Area



PACKAGE DETAILS

SOT-23 SMD Plastic Package



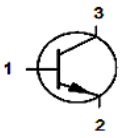
DIM	MIN	MAX
A	1.275	1.325
B	2.40	2.60
C	1.85	1.95
D	2.875	2.925
E	0.57	0.67
F	0.38	0.48
G	3 DEG	
H	–	1.30
J	2.40	2.60
K	7 DEG	
L	0.11	0.13
M	0.58	0.62
N	0.925	0.975
O	0.21	–
P	0.02	0.10
R	–	0.08
S	2 DEG	8 DEG
T	2 DEG	10 DEG

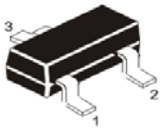
All dimensions are in mm

All Dimensions are in mm

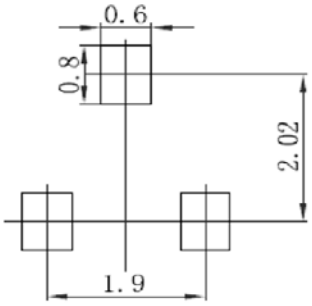
Pin Configuration

1. Base
2. Emitter
3. Collector





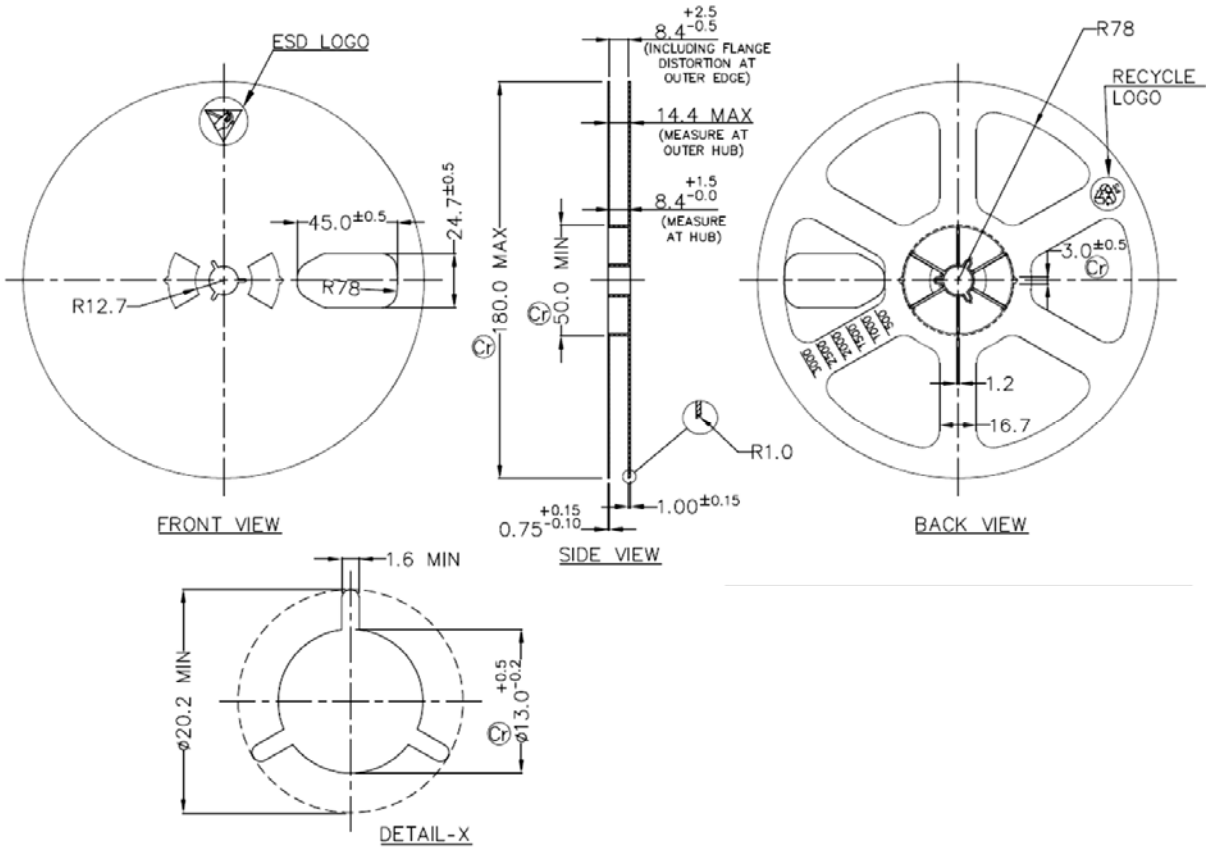
SOT-23 Suggested Pad Layout



Note:
1.Controlling dimension:In millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

BC817_818
Rev04_18102024M

SOT-23 Tape and Reel



Packing Detail

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/Qty	Size	Qty	Size	Qty	Gr Wt
SOT-23 T&R	3K/reel	136 gm/3K pcs	3" x 7.5" x 7.5"	12 K	17" x 15" x 13.5"	192 K	12 kgs
			9" x 9" x 9"	51 K	19" x 19" x 19"	408 K	28 kgs
	10K/reel	415 gm/10K pcs	13" x 13" x 0.5"	10 K	17" x 15" x 13.5"	300 K	16 kgs

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.
Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

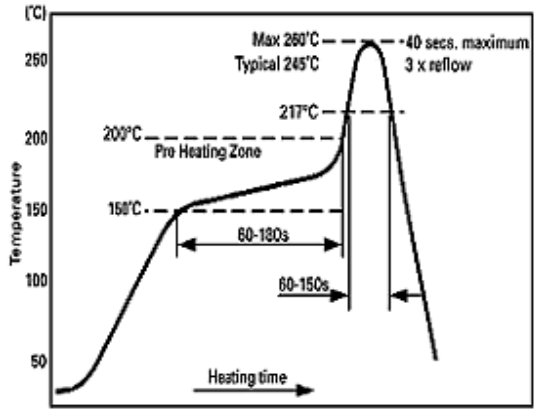
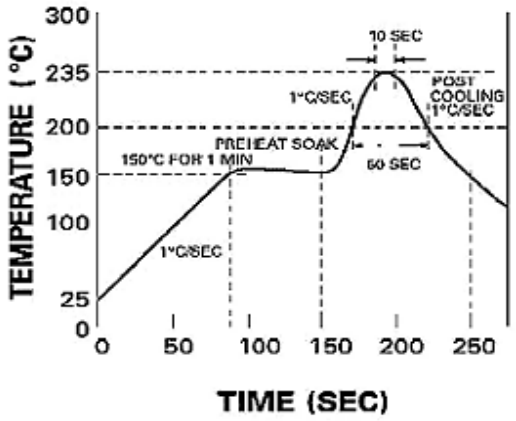


Figure 2

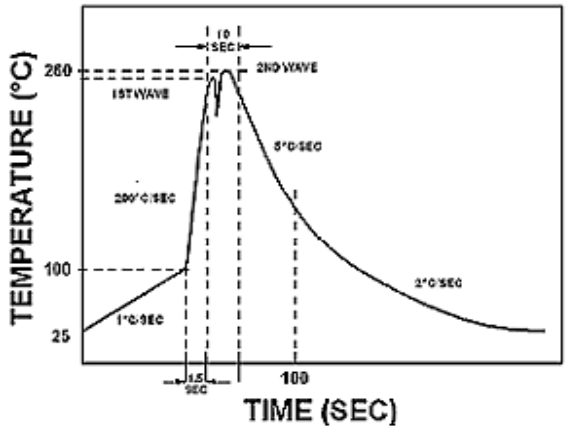


Reflow profiles in tabular form

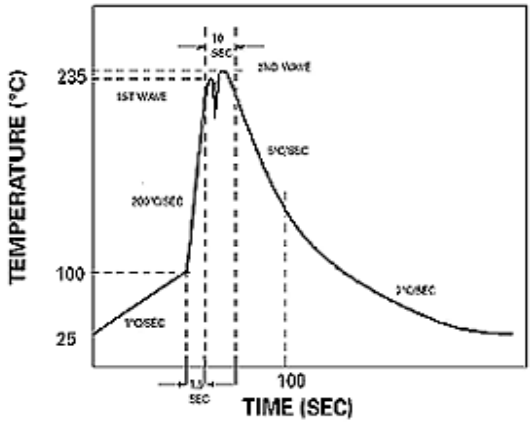
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended Solder Profile For Devices with Pb-free terminal plating where a



The Recommended Solder Profile For Devices with Pb-free terminal plating used with leaded



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.

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BC817_818
Rev04_18102024M